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5	BRS	L5	499	4 and instruction near3 ("32 bits" or 32-bit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/02 10:36	
6	BRS	L6	70	5 and VLIW	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/02 10:37	

Terms used
fetch and **'word length'** and **half word** and **full word** and **aligned** and **sequential** and **address** and **cycle** and **instruction** an

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1 Multiple instruction issue in the NonStop cyclone processor
Robert W. Horst, Richard L. Harris, Robert L. Jardine
May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual internati Architecture**, Volume 18 Issue 3
Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, citings, index ter

This paper describes the architecture for issuing multiple instructions per clock in the NonStop Cyclone Proces and decoded by a dual two-stage prefetch pipeline and passed to a dual six-stage pipeline for execution. Dyna reduce branch penalties. A unique microcode routine for each pair is stored in the large duplexed control store data paths optimized for executing the most frequent instr ...

2 Fitting processors to the needs of a General Purpose Array (EGPA)
Wolfgang Händler, Rainer Klar
September 1975 **Proceedings of the 8th annual workshop on Microprogramming**
Full text available: pdf(781.61 KB) Additional Information: full citation, abstract, references, citings, index ter

1.1 General Purpose Processor The vast majority of contemporary processors can be described as general pur structure often referred to as "von Neumann". 1.2 Associative Array Processor In addition special processors h applications, some involving parallel processing. The associative array processors (AAP) [2] or the synchronou

3 Pipeline Architecture
C. V. Ramamoorthy, H. F. Li
January 1977 **ACM Computing Surveys (CSUR)**, Volume 9 Issue 1
Full text available: pdf(3.53 MB) Additional Information: full citation, references, citings, index terms

4 The Clipper processor: instruction set architecture and implementation
W. Hollingsworth, H. Sachs, A. J. Smith
February 1989 **Communications of the ACM**, Volume 32 Issue 2
Full text available: pdf(4.67 MB) Additional Information: full citation, abstract, references, citings, index ter

Intergraph's CLIPPER microprocessor is a high performance, three chip module that implements a new instruc convenient programmability, broad functionality, and easy future expansion.

5 Compiler-driven cached code compression schemes for embedded ILP processors
Sergei Y. Larin, Thomas M. Conte
November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitect**
Full text available: pdf(1.24 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index ter

h c g e cf c

During the last 15 years, embedded systems have grown in complexity and performance to rival desktop syst systems present unique challenges to processor microarchitecture, including instruction encoding and instruct presents new techniques for reducing embedded system code size without reducing functionality. This approa logic for an embedded VLIW processor in software at system develo ...

6 Associative and Parallel Processors
Kenneth J. Thurber, Leon D. Wald
December 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 4
Full text available: pdf(2.62 MB) Additional Information: full citation, references, citings, index terms

7 Reconfigurable computing: a survey of systems and software
Katherine Compton, Scott Hauck
June 2002 **ACM Computing Surveys (CSUR)**, Volume 34 Issue 2
Full text available: pdf(710.56 KB) Additional Information: full citation, abstract, references, citings, index ter

Due to its potential to greatly accelerate a wide variety of applications, reconfigurable computing has become Its key feature is the ability to perform computations in hardware to increase performance, while retaining mu solution. In this survey, we explore the hardware aspects of reconfigurable computing machines, from single systems, including internal structures and external coupling. W ...

Keywords: Automatic design, FPGA, field-programmable, manual design, reconfigurable architectures, recon systems

8 The architecture of the SPERRY UNIVAC 1100 series systems
B. R. Borgerson, M. D. Godfrey, P. E. Hagerty, T. R. Rykken
April 1979 **Proceedings of the 6th annual symposium on Computer architecture**
Full text available: pdf(841.19 KB) Additional Information: full citation, abstract, references, citings, index ter

This paper presents an overview of the architecture of the SPERRY UNIVAC® 1100 Series systems. The princi formats, main storage and addressing, process management, and I/O.

9 A Conceptual Framework for Computer Architecture
S. S. Reddi, E. A. Feustel
June 1976 **ACM Computing Surveys (CSUR)**, Volume 8 Issue 2
Full text available: pdf(1.82 MB) Additional Information: full citation, references, citings, index terms

10 Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM cu science
William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William B. Kehl, E Navarro, Werner C. Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young
March 1968 **Communications of the ACM**, Volume 11 Issue 3
Full text available: pdf(6.63 MB) Additional Information: full citation, references, citings

Keywords: computer science academic programs, computer science bibliographies, computer science course computer science education, computer science graduate programs, computer science undergraduate program

11 Optimization of instruction fetch mechanisms for high issue rates
Thomas M. Conte, Kishore N. Menezes, Patrick M. Mills, Burzin A. Patel
May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual internat architecture**, Volume 23 Issue 2

Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, references, citings, index ter

Recent superscalar processors issue four instructions per cycle. These processors are also powered by highly-potential performance can only be exploited when fed by high instruction bandwidth. This task is the responsi Accurate branch prediction and low I-cache miss ratios are essential for the efficient operation of the fetch un and branch prediction address this problem. However, these techn ...

12 StaCS: a Static Control Superscalar architecture
Benoît Dupont de Dinechin
December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium** Issue 1-2
Full text available: pdf(1.34 MB) Additional Information: full citation, references, index terms

13 Regular contributions: DSP architectures: past, present and futures
Edwin J. Tan, Wendi B. Heinzelman
June 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 3
Full text available: pdf(1.27 MB) Additional Information: full citation, abstract, references

As far as the future of communication is concerned, we have seen that there is great demand for audio and v signal processing (DSP) is the science that enables traditionally analog audio and video signals to be processe reproduction and manipulation. In this paper, we will explain the various DSP architectures and its silicon imp state-of-the art and examine the issues pertaining to pe ...

14 The Manchester Mark I and atlas: a historical perspective
S. H. Lavington
January 1978 **Communications of the ACM**, Volume 21 Issue 1
Full text available: pdf(945.23 KB) Additional Information: full citation, abstract, references, citings, index ter

In 30 years of computer design at Manchester University two systems stand out: the Mark I (developed over (1956-62). This paper places each computer in its historical context and then describes the architecture and s terminology. Several design concepts such as address-generation and store management have evolved in the The wider impact of Manchester innovations in these and other areas is discu ...

Keywords: Ferranti, ICL, Manchester Mark I, architecture, atlas, compilers, extracodes, index registers, oper storage

15 A low-cost host processor for emulation research
Robert M. McClure
September 1974 **Conference record of the 7th annual workshop on Microprogramming**
Full text available: pdf(355.29 KB) Additional Information: full citation, abstract, references, index terms

Microprogramming has now gained a certain amount of maturity and is a widely used technique in the design exceptions, such as QM-1 by Nanodata, and the D machine and B1700 of Burroughs, the choice of microprogr classic engineering grounds - simplicity and regularity of design, maintainability, flexibility, and cost - rather t research in microprogramming. For the most part, user microprogramm ...

16 The hardware architecture of the CRISP microprocessor
D. R. Ditzel, H. R. McLellan, A. D. Berenbaum
June 1987 **Proceedings of the 14th annual international symposium on Computer architecture**
Full text available: pdf(930.17 KB) Additional Information: full citation, references, citings, index terms

17 Architecture of the IBM system/370
Richard P. Case, Andris Padegs
January 1978 **Communications of the ACM**, Volume 21 Issue 1

Full text available: pdf(2.78 MB) Additional Information: full citation, abstract, references, citings, index ter

This paper discusses the design considerations for the architectural extensions that distinguish System/370 fr some experiences with the original objectives for System/360 and on the efforts to achieve them, and it desc extending the architecture. It covers virtual storage, program control, data-manipulation instructions, timing and monitoring, error handling, and input/output operations. ...

Keywords: architecture, computer systems, error handling, instruction sets, virtual storage

18 Internet nuggets: Internet nuggets

Mark Thorson

June 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 3

Full text available: pdf(699.55 KB) Additional Information: full citation

19 Applications I: A high performance 32-bit ALU for programmable logic

Paul Metzgen

February 2004 **Proceeding of the 2004 ACM/SIGDA 12th international symposium on Field programm**

Full text available: pdf(261.70 KB) Additional Information: full citation, abstract, references, index terms

The Arithmetic-Logic-Unit (ALU) is at the heart of a modern microprocessor, and its size and speed are often processor's cost and performance. This paper presents the design of the ALU used in Altera's NIOS 2.0 soft pr Apex 20KE FPGA architecture. This ALU enabled the 32-bit NIOS 2.0 to consume only 1200 LEs and run at 85 and 70% speed improvement over its predecessor, NIOS 1.1.The Logic-eleme ...

Keywords: ALU, Apex 20KE, FPGA, Nios, programmable logic, soft processors

20 Enhancing the performance of 16-bit code using augmenting instructions

Arvind Krishnaswamy, Rajiv Gupta

June 2003 **ACM SIGPLAN Notices , Proceedings of the 2003 ACM SIGPLAN conference on Languag embedded systems**, Volume 38 Issue 7

Full text available: pdf(276.13 KB) Additional Information: full citation, abstract, references, citings, index ter

In the embedded domain, memory usage and energy consumption are critical constraints. Dual width instruct the ARM provide a 16-bit instruction set in addition to the 32-bit instruction set to address these concerns. Us achieve code size reduction and I-cache energy savings at the cost of performance. We have observed that th exist Thumb instruction pairs that are equivalent to a single ARM instructi ...

Keywords: 16-bit thumb ISA, 32-bit ARM ISA, AX instructions, code size, embedded processor, instruction c